

**Abstract**

A phase detection apparatus is described for use in a phase lock loop (PLL). The apparatus has a first input for a reference signal, a second input for a loop feedback signal and an output  
5 for the phase difference signal. Two D-type flip-flops are provided, the first being clocked with the reference signal and the second with the loop feedback signal. Means are provided to delay the output of the second flip-flop relative to the first flip-flop, thereby effecting minimal overlap, when using the phase detection apparatus in a fractional- N phase lock loop, of the interpolator activity with that of the charge pump.